MONTROSE COMPLIANCE SERVICES, INC.
ELECTROMAGNETIC COMPATIBILITY AND PRODUCT SAFETY
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Mark I. Montrose

Mark Montrose is principal consultant and owner of Montrose Compliance Services, Inc., a full-service regulatory compliance firm specializing in electromagnetic compatibility (EMC). Prior to becoming a consultant and expert witness, Mark was responsible for regulatory compliance at several large high technology companies in the Silicon Valley Region of California. These companies include Zilog, Alcatel Information Systems, Wyse Technology, Whittaker Communications and MIPS Computer Systems among others.

Mr. Montrose has 45 years of experience as a consultant, trainer, systems designer, product engineer, manufacturing engineer and component engineer in addition to being an expert witness for different legal matters. He held management positions in both regulatory compliance and engineering services.

Expertise includes design, test and certification of Information Technology as well as Industrial, Scientific and Medical Equipment associated with EMC to ensure compatibility is achieved. Every electrical product that exists utilizes electromagnetic energy. Electromagnetic is the physics behind electrical engineering.

Consulting services include comprehensive design analysis for printed circuit boards at the schematic and component level to achieve signal integrity and electromagnetic compatibility, as well as end-system integration based on environment of use.

Montrose Compliance Services is assessed as an EMC test laboratory (IEC/ISO 17025:2017) for companies wishing to enter the European market using the Technical File route, and is also both an Exemplar Global (*iNARTE*) Accredited EMC Test Laboratory and a certificated Master EMC Design Engineer.

Education

California Polytechnic State University (1979), San Luis Obispo, California

- Bachelor Degree - Electrical Engineering
- Bachelor Degree - Computer Science

Santa Clara University (1983), Santa Clara, California

- Master's Degree - Engineering Management

Professional activities are within the IEEE. His involvement includes the following *abbreviated list*:

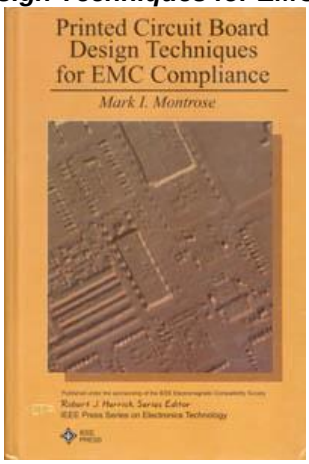
- Life Senior Member of the IEEE
- Past Division VI Director and *Member of the Board of Directors of the IEEE (2009-2010)*
- Past long-term member - Board of Directors of the IEEE Electromagnetic Compatibility Society (EMCS)
- Founder and First President - IEEE Product Safety Engineering Society (PSES)
- Co-Founder – IEEE Systems Council
- Co-Founder – IEEE Nanotechnology Council
- Past member – IEEE Technical Activity Board

Mark has authored and presented numerous technical papers on sophisticated printed circuit board and system design, theory and layout related to all aspects of EMC and signal integrity at IEEE International EMC Symposiums and Colloquiums worldwide. He is also published in the *Transactions of the IEEE EMC Society*. Mark presents tutorials and workshops at international conferences as an invited speaker. He also provides seminars to corporate clients that includes hands-on training, testing and troubleshooting related to any aspect of EMC and system design. For fifteen years, Mark was an instructor for the University of California Santa Cruz extension program.

Mr. Montrose authored five best-selling reference/textbooks sold internationally. Most books are published under sponsorship of the IEEE EMC Society with translation into Chinese, Japanese and Korean through John Wiley & Sons, plus self-publishing his last book *EMC Made Simple*.

Publications – Textbooks for practicing engineers without a formal college education

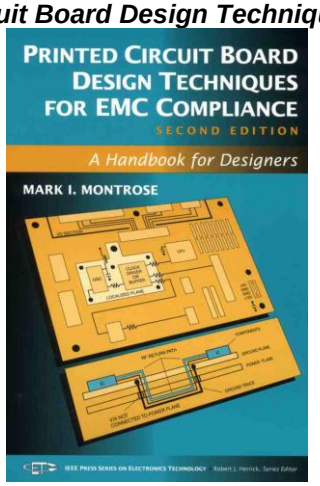
- ***Printed Circuit Board Design Techniques for EMC Compliance.*** **1st ed.–1995**



English

Japanese

- ***Printed Circuit Board Design Techniques for EMC Compliance*** **2nd ed.–2000**



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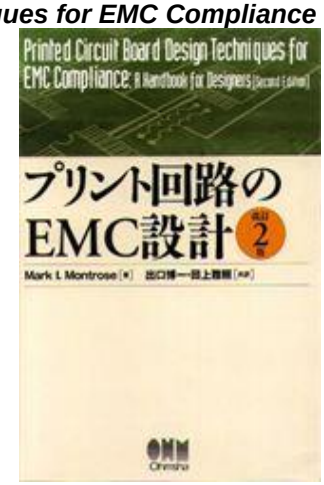

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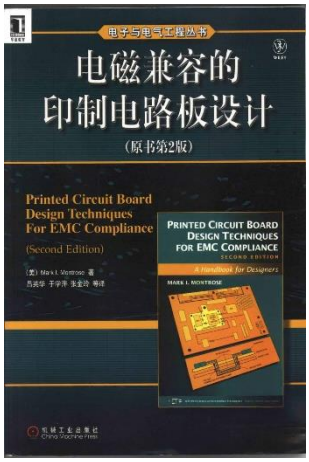
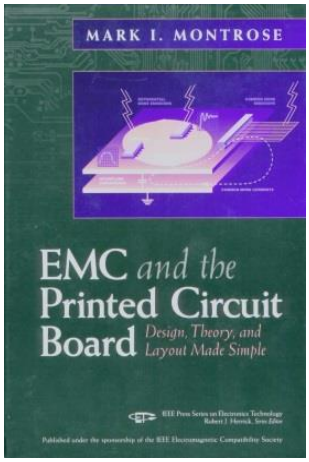


Chinese

- ***EMC and the Printed Circuit Board - Design, Theory and Layout Made Simple.*** **1999**



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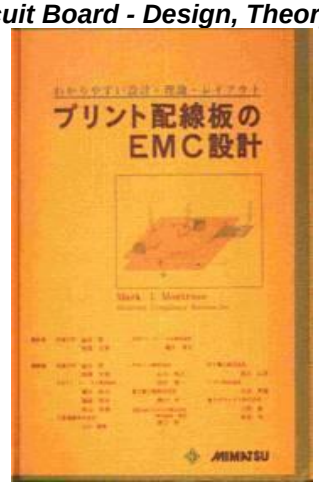

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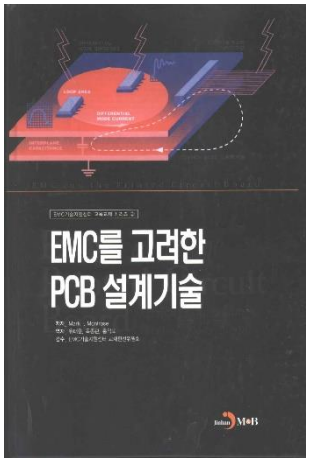
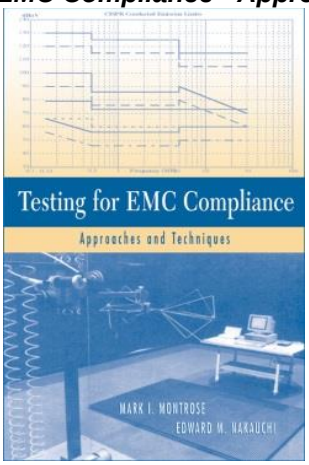


Korean

- ***Testing for EMC Compliance - Approaches and Technique.*** **2004**



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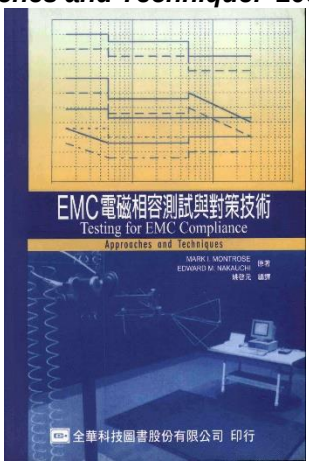
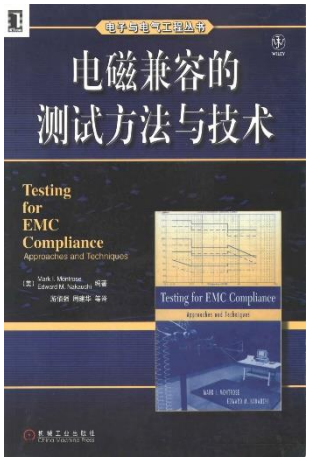
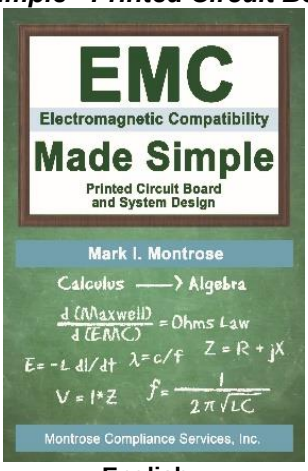


Traditional Chinese (Taiwan)



Simplified Chinese (Mainland)

- ***EMC Made Simple - Printed Circuit Board and System Design.*** **2014**



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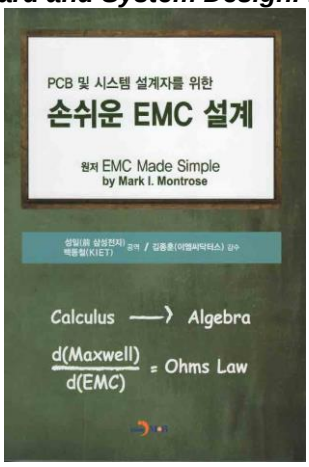
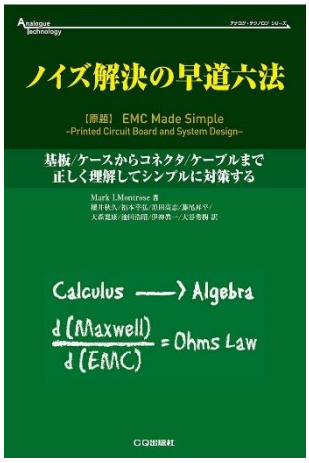


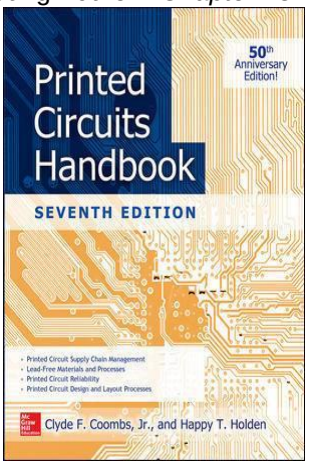
Korean



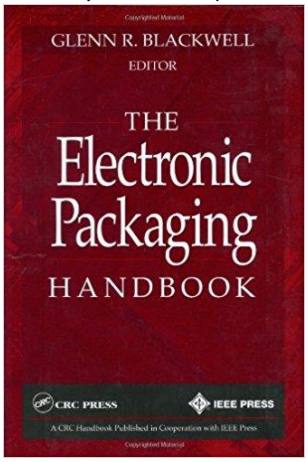
Japanese

Engineering reference books (contributing author)

Printed Circuit Handbook
(Clyde Coombs Primary Editor).
Contributing Author - *Chapter 15*. McGraw Hill, 2016.



Electronics Packaging Handbook
Contributing Author-*Chapter 6*.
IEEE Press/CRC Press, 2000.



Assessments and Certifications

EMC Master Design Engineer

EMC Accredited Test Laboratory

ISO/IEC 17025 International EMC Test Laboratory Assessment

Certificate of Assessment

Presented by

Dr.-Ing. Diethard Hansen
ISO/IEC 17025 Laboratory Assessor
EURO EMC SERVICE (EES) Dr. Hansen Consulting
CH-8965 Berikon, Bahnhofstr. 39, Switzerland

to

Montrose Compliance Services, Inc.
2353 Mission Glen Dr.
Santa Clara, California 95051-1214, USA

In my opinion, Montrose Compliance Services, Inc. complies with the requirements of ISO/IEC 17025: 2017 Ed. 3, "*General requirements for the competence of testing and calibration laboratories.*"

This assessment demonstrates technical competence and operation of the company along with an appropriate Quality Management System for the scope and locations described in the accompanying schedule that forms an essential part of this certificate.

Certificate Number: US-2022-01

Dr.-Ing. Diethard Hansen

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Technical Papers Published and Presented at International Conferences – IEEE EMC Society

1. “Analysis on the Effectiveness of Clock Trace Termination Methods and Trace Lengths on a Printed Circuit Board”. IEEE Int’l Symposium on EMC, 1996. pp. 453-458
2. “Analysis on the Effectiveness of Image Planes on a Printed Circuit Board”. IEEE Int’l Symposium on EMC, 1996. pp. 326-331
3. “Time and Frequency Domain Analysis for Right Angle Corners on Printed Circuit Board Traces”. IEEE Int’l Symposium on EMC, 1998. pp. 551-556
4. “Right Angle Corners on Printed Circuit Board Traces, Time and Frequency Domain Analysis”. EMC’99 Tokyo, pp.638-641
5. “Analysis on Loop Area Trace Radiated Emissions from Decoupling Capacitor Placement on Printed Circuit Boards”. IEEE Int’l Symposium on EMC, 1999. pp. 423-428
6. “Analysis on the Effectiveness of the 20-H Rule Using Numerical Simulation Technique”. IEEE Int’l Symposium on EMC, 2002. pp. 328-333
7. “Product Safety and the Heat Sink – Dilemma of Minimizing Radiated Emissions and Maximizing Thermal Cooling”. IEEE Int’l Symposium on EMC, 2003. pp. 134-137
8. “Analysis on the Effectiveness of Printed Circuit Board Edge Termination Using Discrete Components Instead of Implementing the 20-H Rule”. IEEE Int’l Symposium on EMC, 2004. pp. 45-5
9. “Analysis on the Effectiveness of High Speed Printed Circuit Board Edge Radiated Emissions Based on Stimulus Source Location”. IEEE Int’l Symposium on EMC, 2004. pp. 326-331
10. “Radiated Emission Analysis from Printed Board Edges Using Multiple Stimulus Sources”. 17th Int’l Zurich Symposium on EMC, 2006. pp. 574-577
11. “Power and Ground Bounce Effects on Component Performance Based on Printed Circuit Board Edge Termination Methodologies”. IEEE Int’l Symposium on EMC, 2007
12. “Radiated Emission Effects from Multiple Via Stimulation Within a Printed Circuit Board. Asia-Pacific Symposium on EMC & 19th Int’l Zurich Symposium on EMC 2008. pp. 176-179
13. “Component Performance Associated with Power/Return Plane Bounce Using Board Edge Termination”. EMC Society of Australia EMC Conference. 2010
14. “Radiated Emission Far-Field Propagation with Multiple Ground Stitch Ground Locations Within a Printed Circuit Board”. 2010 Asia-Pacific Int’l Symposium on EMC. pp. 297-300
15. “How Decoupling Capacitors May Cause Radiated EMI”. EMC Society of Australia EMC Conference. 2011

Journal Papers Published in the Transactions of the IEEE EMC Society

1. **“**Analysis on the Effectiveness of the 20-H Rule for Printed Circuit Board Layout to Reduce Edge-Radiated Coupling**”**. IEEE Transactions on EMC, May 2005. Vol. 47, No. 2. pps. 227-233
2. **“**Voltage and Return Plane Bounce Affecting Digital Components Using Different Printed Circuit Board Edge Termination Methodologies**”**. IEEE Transactions on EMC, August 2011, Vol. 53, No. 3. pps. 802-805